What is Claimed is:

[c1] An apparatus for maintaining signal integrity between integrated circuits residing on a printed circuit board, said apparatus comprising:

adjustable delay circuitry within said circuits, said adjustable delay circuitry being adapted to adjust timing of signals processed within said circuits

;

a phase monitor connected to said circuits, said phase monitor being adapted to detect phase differences between signals output by said circuits; and

a controller connected to said delay circuitry and said phase monitor, said controller being adapted to adjust said delay circuitry to compensate for said phase differences.

[c2] The apparatus in claim 1, further comprising:

first data lines connecting said circuits to each other; and

second data lines connecting said controller to said circuits,

wherein said second data lines transmit data at a slower rate than said first data lines.

[c3] The apparatus in claim 1, further comprising a serial data line connecting said controller to said circuits.

[c4] The apparatus in claim 1, wherein at least one of said circuits comprises a receiver circuit, said receiver circuit comprising:

a plurality of channels; and

a configuration word interface connected to said channels and to said controller,

wherein said adjustable delay circuitry comprises at least one adjustable delay device within each of said channels, and

wherein said configuration word interface controls said delay device to coordinate a signal timing of said channels.

[c5] The apparatus in claim 4, further comprising delay registers between said delay device and said configuration word interface, wherein said delay registers are

adapted to store information regarding timing delay of an associated delay device.

[c6] The apparatus in claim 4, wherein said configuration word interface is connected to said controller and said controller is adapted to supply information to control said delay device.

[c7] The apparatus in claim 4, wherein said configuration word interface permits dynamic control of said delay device.

[c8] The apparatus in claim 4, wherein said configuration word interface includes a phase voltage converter.

[c9] The apparatus in claim 4, wherein said adjustable delay device comprises:

a resistor-capacitor network;

a Schmitt trigger connected to said resistor-capacitor network; and

a digital-to-analog converter connected to said resistor-capacitor network.

[c10] The apparatus in claim 4, wherein said adjustable delay device comprises:

a resistor-capacitor network;

variable transistors connected to said resistor-capacitor network; and

a digital-to-analog converter connected to said resistor-capacitor network.

[c11] A receiver circuit comprising:

a plurality of channels; and

a configuration word interface connected to said channels, wherein each of said channels comprises at least one adjustable delay device,

wherein said configuration word interface controls said delay device to coordinate a signal timing of said channels.

[c12] The receiver circuit in claim 11, further comprising delay registers connected between said delay device and said configuration word interface, wherein said delay registers are adapted to store information regarding an individual timing delay of an associated delay device.

[c13] The receiver circuit in claim 11, wherein said configuration word interface is connected to an external controller that supplies information to control said delay device.

[c14] The receiver circuit in claim 11, wherein said adjustable delay device and said configuration word interface are positioned on a single printed circuit board.

[c15] The receiver circuit in claim 11, wherein said configuration word interface permits dynamic control of said delay device.

[c16] The receiver circuit in claim 11, wherein said configuration word interface includes a phase voltage converter.

[c17] The receiver circuit in claim 11, wherein said delay circuitry comprises:

a resistor-capacitor network;

a

Schmitt trigger connected to said resistor-capacitor network; and

a digital-to-analog converter connected to said resistor-capacitor network.

[c18] The receiver circuit in claim 11, wherein said adjustable delay device comprises:

a resistor-capacitor network;

variable transistors connected to said resistor-capacitor network; and

a digital-to-analog converter connected to said resistor-capacitor network.

[c19] A method of coordinating timing signals within circuits on a printed circuit board, said method comprising:

detecting phase differences between signals output by said circuits using a phase monitor; and

adjusting delay circuitry within said circuits to compensate for said phase differences using a controller.

[c20] The method in claim 19, wherein first data lines connecting said controller to said circuits transmit data at a slower rate than second data lines connecting said circuits to each other.

[c21] The method in claim 19, further comprising using a serial data line to connect said controller to said circuits

[c22] The method in claim 19, wherein at least one of said circuits comprises a receiver circuit, and said adjusting process comprises transmitting control information from said controller through a configuration word interface to said delay devices to coordinate a signal timing of said channels.

[c23] The method in claim 22, further comprising dynamically controlling said delay circuitry using said configuration word interface.

[c24] The method in claim 19, further comprising storing delay information in delay registers.